REMARKS

The non-final Office Action mailed February 8, 2005, has been reviewed and carefully considered. Claims 1, 9, 10, 12-16, 25-29, 32 and 37-44 have been amended and claims 11 and 24 have been canceled. Claims 1-10, 12-23 and 35-44 are pending. Applicants appreciate Examiner's indication of allowability of claims 5-15, 20-27, and 33-43.

In paragraph 2 on page 2 of the Office Action, the drawings were objected to due to certain informalities.

Applicants respectfully traverse the objection to the drawings. However, in order to advance prosecution of Applicants' Application, Applicants are included a replacement drawing sheet identifying Fig. 3 as prior art.

In paragraph 4 on page 3 of the Office Action, claims 1, 2, 16-17, 28, and 44 were rejected under § 103(a) over Reed et al. (U.S. Patent No. 5,961,658) in view of Krishnapura et al. (U.S. Patent No. 6,717,461). In paragraph 5 on page 5 of the Office Action, claims 3, 4, 18, and 19 were rejected under § 103(a) over Reed in view of Krishnapura, further in view of Lee et al. (U.S. Patent No. 6,148,431). In paragraph 6 on page 7 of the Office Action, claims 29 and 30 were rejected under § 103(a) over Sawaguchi et al. (U.S. Patent Pub. No. 2002/0040462) in view of Reed, further in view of Krishnapura. In paragraph 7 on page 9 of the Office Action, claims 31 and 32 were rejected under § 103(a) over Sawaguchi in view of Reed, further in view of Krishnapura.

Applicants respectfully traverse the § 103(a) rejections, but in the interest of expediting prosecution have amended independent claims to include an offset term that is provided specific for each sequence selection stage to produce an error sequence, wherein the offset terms comprise an offset threshold dependent upon the sequence at the output of the Viterbi decoder.

In contrast, Reed only discloses thresholds in the context of a slicer. Reed states at column 7, lines 33-35 that "A slicer generates estimated sample values simply by comparing the channel samples to programmable positive and negative thresholds according to Table 2." Referring to the Summary at column 4, lines 33-37, Reed states "channel samples are initially equalized into a PR4 partial response so that a simple slicer circuit can generate estimated sample values. The PR4 equalized channel samples are then passed through a 1+D filter to generate EPR4 equalized channel samples which are processed by an EPR4 Viterbi sequence

detector to generate a preliminary binary sequence." Therefore, only channel samples are thresholded, and Reed fails to disclose, teach, or suggest that "the sequence selection stage and the Viterbi decoder each include at least one threshold." Moreover, Reed fails to suggest an offset term that is provided specific for each sequence selection stage to produce an error sequence, wherein the offset terms comprise an offset threshold dependent upon the sequence at the output of the Viterbi decoder.

Krishnapura fails to remedy the deficiencies of Reed. Krishnapura does not even mention a Viterbi decoder or a sequence selection stage. Moreover, Krishnapura fails to suggest an offset term that is provided specific for each sequence selection stage to produce an error sequence, wherein the offset terms comprise an offset threshold dependent upon the sequence at the output of the Viterbi decoder.

Additionally, Applicants require "a sequence selection stage for . . . selecting a sequence based upon the analysis of error events."

Reed, in contrast, is concerned with correcting preliminary binary sequences and states at column 4, lines 53-37, "When an error is detected in the preliminary binary sequence (e.g., a peak error event is detected or an error syndrome of an error detection code (EDC) indicates an error), an error corrector corrects the error in the preliminary binary sequence and generates a corrected output sequence." Because Reed focuses on correcting preliminary binary sequences and does not select sequences, Reed fails to disclose, teach or suggest "a sequence selection stage for . . . selecting a sequence based upon the analysis of error events."

Krishnapura fails to remedy the deficiencies of Reed. Krishnapura does not even mention a sequence selection stage.

Lee, and Sawaguchi too fail to remedy the deficiencies of Reed and fail to remedy the deficiencies of Krishnapura. Neither Lee nor Sawaguchi disclose, teach or suggest "a sequence selection stage for . . . selecting a sequence based upon the analysis of error events," and that "the sequence selection stage and the Viterbi decoder each include at least one threshold." Moreover, Lee, and Sawaguchi, alone or in combination with Reed and/or Krishnapura, fail to suggest an offset term that is provided specific for each sequence selection stage to produce an error sequence, wherein the offset terms comprise an offset threshold dependent upon the sequence at the output of the Viterbi decoder.

Reed, Krishnapura, Lee, and Sawaguchi alone or in combination, fail to disclose, teach or suggest all of the limitations of Applicants' application. Thus the § 103(a) rejections are also improper. Accordingly, Applicants request that the Section 103 rejections be withdrawn.

Furthermore, with respect to the § 103(a) rejections, Krishnapura states with respect to dynamic bias, that "dynamic bias can be applied to the band-pass output," column 9, line 7, and that "dynamic biasing can be applied to circuits such as the filter of FIG. 8a," column 11, line 7. The filter of Fig. 8a is a first-order, log-domain, low-pass filter, column 9, lines 66-67. However, the connection between Krishnapura and Reed is attenuated. This is because Krishnapura does not even disclose an at least one sequence selection stage threshold, or an at least one Viterbi decoder threshold. The mere fact that Krishnapura teaches dynamically biasing filtered data does not indicate that Krishnapura and Reed are combinable.

MPEP 706.01(j) states that to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references when combined must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

There is no indication that the combination of Reed with Krishnapura would be successful. Reed teaches in the Summary at column 4, lines 38-50 that "The preliminary binary sequence is remodulated into an estimated or ideal PR4 sample sequence which is subtracted from the PR4 equalized channel samples to generate an error sample sequence. An error pattern detector processes the error sample sequence to detect the dominant error events associated with the EPR4 Viterbi sequence detector. For the data densities of interest (user bit densities of 1.8 to 2.5), the most dominant error event (1,-1 in SNRZI space) is best detected in the EPR4 domain, and the next most dominant error event (1,-2,2,-1 in SNRZI space) is best detected in the PR4 domain. Thus, the error pattern detector comprises a plurality of finite-impulse-response (FIR) filters matched to the dominant error events and, specifically, a first FIR filter matched the error event in EPR4 space, and a second FIR filter matched to the error event in PR4 space. When an

error is detected in the preliminary binary sequence (e.g., a peak error event is detected or an error syndrome of an error detection code (EDC) indicates an error), an error corrector corrects the error in the preliminary binary sequence and generates a corrected output sequence." In Reed, the FIR filters of the error pattern detector are subsequently used when errors are detected in the preliminary binary sequence in order to correct the errors in the preliminary binary sequence. Applying dynamic biasing to the FIR filters would serve to defeat the intended purpose of the FIR filters because reducing noise in the FIR filters, would result in corrected preliminary binary sequence without noise correction, e.g., FIR filters corrected for noise that are used to correct preliminary binary sequences would result in not filtering out noise in the preliminary binary sequences. Therefore, Reed and Krishnapura are not easily combinable.

The alleged motivation for modifying Reed with Krishnapura is conclusory, based on hindsight and therefore, improper. The alleged motivation is "because it would provide such system with the enhanced capability of providing noise reduction for small input signals, thus showing the external linearity and syllabic companding of the dynamically biased filter (col. 14, lines 1-5 of Krishnapura et al.)." This alleged motivation merely states a function of dynamic biasing. No clear and particular evidence is provided that would motivate one to modify Reed's system. Reed's system is presumably adequate for its intended purpose, and no evidence is provided to indicate any deficiencies in Reed's system. Thus, the alleged motivation is merely a reconstruction of the claim limitations based on hindsight.

Dependent claims 2-10, 12-15, 17-23, 25-27 and 30-43 are also patentable over the references, because they incorporate all of the limitations of the corresponding independent claims 1, 16 and 29 respectively. Further dependent claims 2-10, 12-15, 17-23, 25-27 and 30-43 recite additional novel elements and limitations. Applicants reserve the right to argue independently the patentability of these additional novel aspects. Therefore, Applicants respectfully submit that dependent claims 2-10, 12-15, 17-23, 25-27 and 30-43 are patentable over the cited references, and request that the objections to the independent claims be withdrawn.

On the basis of the above amendments and remarks, it is respectfully submitted that the claims are in immediate condition for allowance. Accordingly, reconsideration of this application and its allowance are requested. Please charge/credit Deposit Account No. 50-0996 (HITG.047PA) for any deficiencies/overpayments.

If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicant's attorney of record, David W. Lynch at 651-686-6633 Ext 116.

Respectfully submitted,

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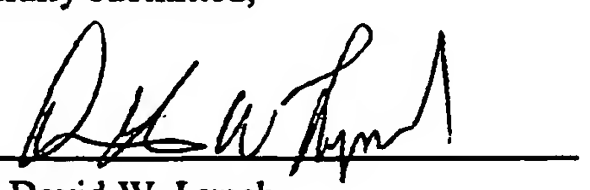
By: 
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